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Question No: 1 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

- ► **All of the inputs are one (Page 40)**
- ► Any of the input is one
- ► Any of the input is zero
- ► All the inputs are zero

Question No: 2 (Marks: 1) - Please choose one
The OR Gate performs a Boolean _____ function

- ► **Addition (Page 42) rep**
- ► Subtraction
- ► Multiplication
- ► Division

Question No: 3 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

- ► **True rep Click here for Detail**
- ► False

Question No: 4 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

- ► A > B = 1, A < B = 0, A < B = 1
- ► A > B = 0, A < B = 1, A = B = 0
- ► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
- ► **A > B = 0, A < B = 1, A = B = 1**

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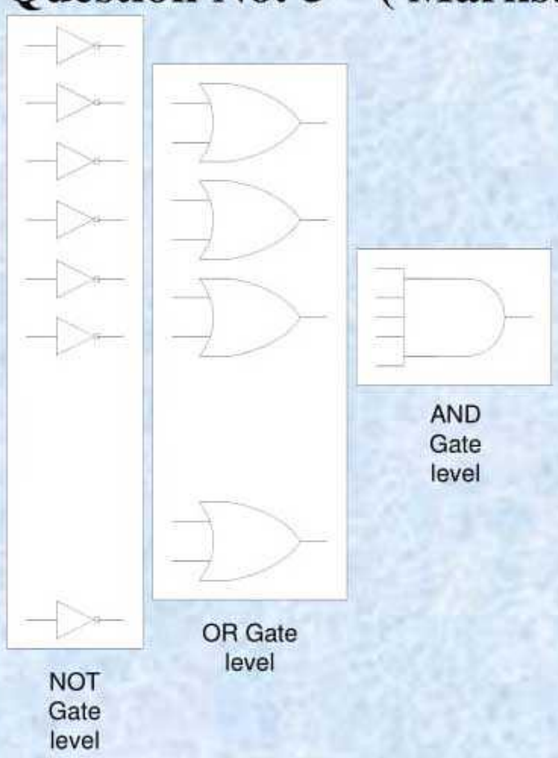
Question No: 5 (Marks: 1) - Please choose one

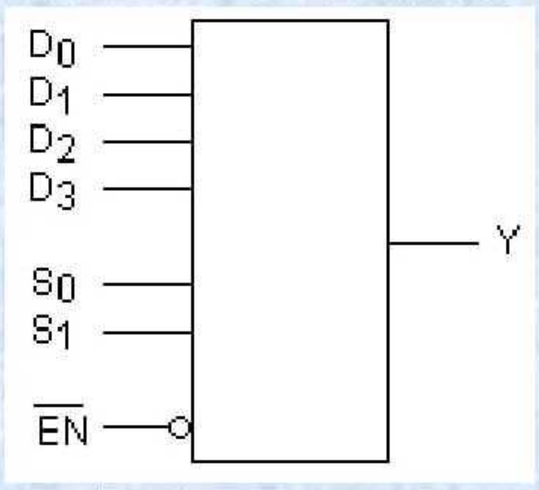


The diagram above shows the general implementation of _____ form

- boolean
- arbitrary
- **POS (Page 122)**
- SOP

Question No: 6 (Marks: 1) - Please choose one

The device shown here is most likely a



- Comparator
- **Multiplexer Click here for detail**
- Demultiplexer
- Parity generator

Question No: 7 (Marks: 1) - Please choose one

Demultiplexer converts _____ data to _____ data

- Parallel data, serial data
- **Serial data, parallel data (Page 356)**
- Encoded data, decoded data
- All of the given options.

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Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____
- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228) rep**
- ► Bi-stable singlevibrators

Question No: 9 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
- ► 0
- ► **1 (Page 230)**
- ► Invalid
- ► Input is invalid

Question No: 10 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
- ► 0
- ► 1
- ► **Invalid (Page 230)**
- ► Input is invalid

Question No: 11 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 12 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 13 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

- ► Using S-R Flop-Flop
- ► D-flipflop
- ► **J-K flip-flop (Page 252)**
- ► T-Flip-Flop

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Question No: 14 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock
- ► True
- ► **False (Page 245)**

Question No: 15 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 16 (Marks: 1) - Please choose one
A negative edge-triggered flip-flop changes its state **when** _____
- ► Enable input (EN) is set
- ► Preset input (PRE) is set
- ► Low-to-high transition of clock
- ► **High-to-low transition of clock (Page 228)**

Question No: 17 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
- ► 10 mW
- ► **25 mW (Page 242)**
- ► 64 mW
- ► 1024

Question No: 18 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
- ► Race condition
- ► **Clock Skew (Page 226) rep**
- ► Ripple Effect
- ► None of given options

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
- ► 3
- ► 7
- ► **8 (Page 272) rep**
- ► 15

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Question No: 20 (Marks: 1) - Please choose one
A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

- ► 10 Hz
- ► **50 Hz (Page 298)**
- ► 100 Hz
- ► 500 Hz

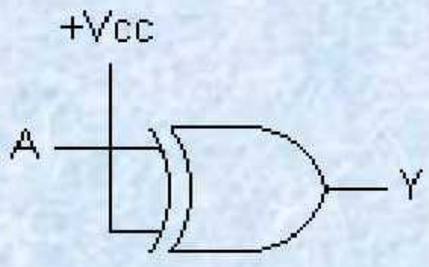
Question No: 21 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319)**

Question No: 22 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

- ► 3
- ► **4 (Page 281) rep**
- ► 7
- ► 10

Question No: 23 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for Detail rep**
- ► $\overline{A}$

Question No: 24 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

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Question No: 25 (Marks: 1) - Please choose one

In _____ the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

- ► Moore machine
- ► Meally machine
- ► **Johnson counter (Page 354)**
- ► Ring counter

Question No: 26 (Marks: 1) - Please choose one

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

- ► Moore machine
- ► Meally machine
- ► Johnson counter
- ► **Ring counter (Page 355) rep**

Question No: 27 (Marks: 1) - Please choose one

Which is not characteristic of a shift register?

- ► **Serial in/parallel in (Page 346)**
- ► Serial in/parallel out
- ► Parallel in/serial out
- ► Parallel in/parallel out

Question No: 28 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► **1100**
- ► 0011
- ► **0000 Click here for detail rep**
- ► 1111

Question No: 29 (Marks: 1) - Please choose one

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

- ► Write Time
- ► Recycle Time
- ► Refresh Time
- ► **Access Time (Page 417) rep**

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Question No: 30 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

- n+2 (n plus 2)
- **2n (n multiplied by 2) (Page 354) rep**
- 2^n (2 raise to power n)
- n^2 (n raise to power 2)

Question No: 1 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

- FALSE
- **TRUE (Page 250)**

Question No: 2 (Marks: 1) - Please choose one
The output of an XNOR gate is 1 when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

- I Only
- IV Only
- I and IV only
- **II and III only (Page 53)**

Question No: 3 (Marks: 1) - Please choose one
NAND gate is formed by connecting _____

- **AND Gate and then NOT Gate (Page 45)**
- NOT Gate and then AND Gate
- AND Gate and then OR Gate
- OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

- Zero
- **One (Page 46)**
- Undefined
- No output as input is invalid

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Question No: 5 (Marks: 1) - Please choose one
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

- ► Radiation-Erase programming method (REPM)
- ► **In-System Programming (ISP) (Page 194)**
- ► In-chip Programming (ICP)
- ► Electronically-Erase programming method(EEPM)

Question No: 6 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

- ► !
- ► &
- ► **# (Page 201) rep**
- ► $

Question No: 7 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

- ► 0
- ► 1
- ► **Invalid (Page 230) rep**
- ► Input is invalid

Question No: 8 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 9 (Marks: 1) - Please choose one
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

- ► 0
- ► **1 (Page 227) rep**
- ► Q(t)
- ► Invalid

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

- ► True
- ► **False (Page 245) rep**

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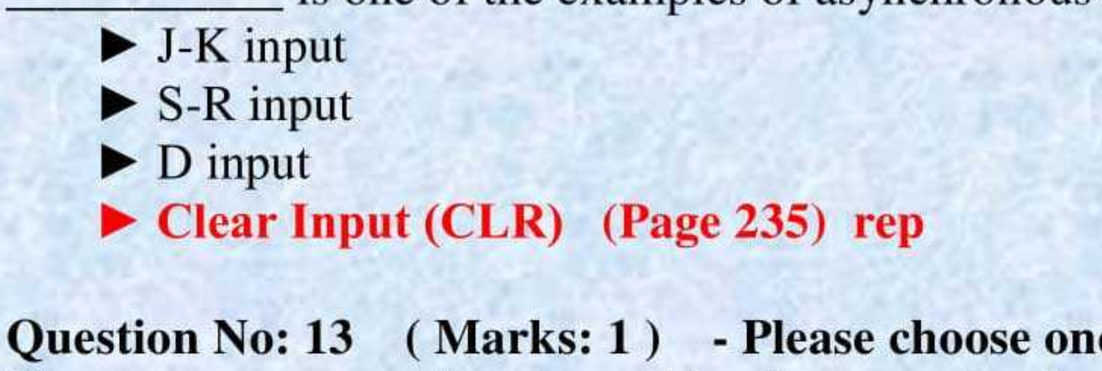
Question No: 11 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 12 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.
- ► J-K input
- ► S-R input
- ► D input
- ► **Clear Input (CLR) (Page 235) rep**

Question No: 13 (Marks: 1) - Please choose one
The _____ input overrides the _____ input
- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 14 (Marks: 1) - Please choose one
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



- ► AND
- ► NAND
- ► NOR
- ► **XNOR (Page 262)**

Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the combination of current state and inputs.

- ► **Mealy machine (Page 332)**
- ► Moore Machine
- ► State Reduction table
- ► State Assignment table

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Question No: 16 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335) rep**

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► **Parallel data to serial (Page 356) rep**
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 19 (Marks: 1) - Please choose one
In the following statement
Z PIN 20 ISTYPE 'reg.invert';
The keyword "reg.invert" indicates _____

- ► An inverted register input
- ► An inverted register input at pin 20
- ► Active-high Registered Mode output
- ► **Active-low Registered Mode output (Page 360)**

Question No: 20 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

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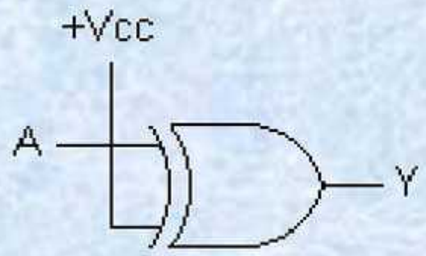
Question No: 21 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- 1
- 0
- **A Click here for detail rep**
- $\overline{A}$

Question No: 22 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- 2
- 4
- 6
- **8 (not sure) rep**

Question No: 23 (Marks: 1) - Please choose one
A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/$\overline{\text{LEFT}}$ input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

- 1110
- 0111
- 1000
- **1001 Click he re for detail**

Question No: 24 (Marks: 1) - Please choose one
The high density FLASH memory cell is implemented using _____

- **1 floating-gate MOS transistor (Page 419) rep**
- 2 floating-gate MOS transistors
- 4 floating-gate MOS transistors
- 6 floating-gate MOS transistors

Question No: 25 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- Read Only Memory
- **Fist In First Out Memory (Page 425)**
- Flash Memory
- Fast Page Access Mode Memory

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Question No: 26 (Marks: 1) - Please choose one

If the FIFO Memory output is already filled with data then _____

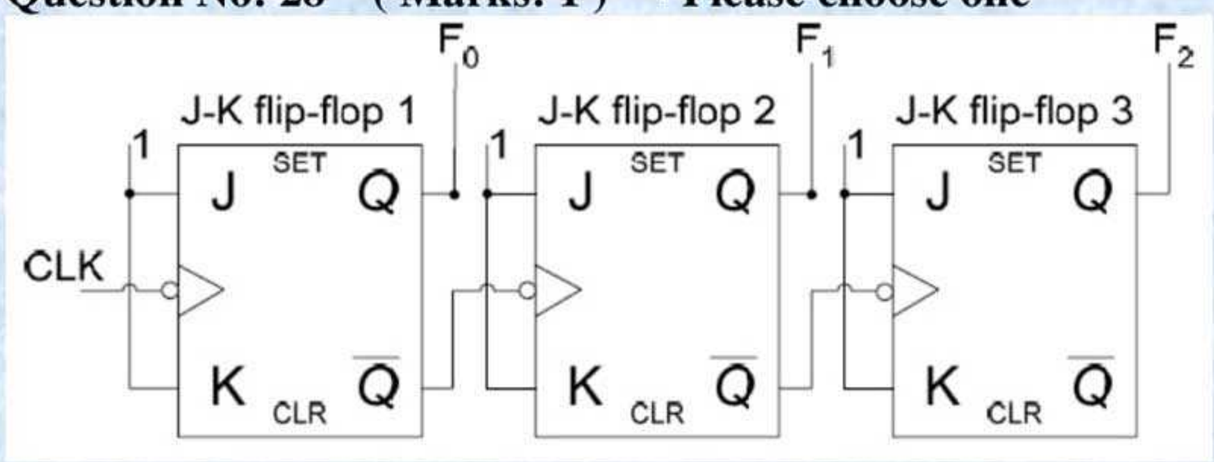
- ► It is locked; no data is allowed to enter
- ► It is not locked; the new data overwrites the previous data.
- ► Previous data is swapped out of memory and new data enters
- ► **None of given options**

Question No: 27 (Marks: 1) - Please choose one

The process of converting the analogue signal into a digital representation (code) is known as _____

- ► Strobing
- ► Amplification
- ► **Quantization (Page 445)**
- ► Digitization

Question No: 28 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270) rep**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 29 (Marks: 1) - Please choose one

$(A + B)(A + \overline{B} + C)(\overline{A} + C)$ is an example of _____

- ► **Product of sum form (Page 77)**
- ► Sum of product form
- ► Demorgans law
- ► Associative law

Question No: 30 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

- ► Q2:= Q1 $ X $ Q3
- ► **Q2:= Q1 # X # Q3 (Page 210)**
- ► Q2:= Q1 & X & Q3
- ► Q2:= Q1 ! X ! Q3

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Question No: 1 (Marks: 1) - Please choose one
Caveman number system is Base _____ number system

► 2
► **5 (Page 11)**
► 10
► 16

Question No: 2 (Marks: 1) - Please choose one
The output of an XOR gate is zero (0) when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 3 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____**10001(right opt is not given)**

► 11101
► 11011
► **10111 (According to rule) rep**
► 11110

Question No: 4 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True Click here for Detail rep**
► False

Question No: 5 (Marks: 1) - Please choose one
The simplest and most commonly used Decoders are the _____ Decoders
► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

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Question No: 6 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 7 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

► **True (Page 161)**
► False

Question No: 8 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 9 (Marks: 1) - Please choose one
If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245) rep**

Question No: 11 (Marks: 1) - Please choose one
The low to high or high to low transition of the clock is considered to be a(n) _____

► State
► **Edge (Page 228)**
► Trigger
► One-shot

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Question No: 12 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 13 (Marks: 1) - Please choose one
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 14 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
► Ten
► Eight
► Three
► **Two (Page 262) rep**

Question No: 15 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 255) rep**

Question No: 16 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 17 (Marks: 1) - Please choose one
A transparent mode means _____

► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

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Question No: 18 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 19 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356) rep**
► Serial in / Parallel out shift register
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 20 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356) rep**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 21 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 22 (Marks: 1) - Please choose one
Smallest unit of binary data is a _____

► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 23 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394) rep**
► 8
► 16

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Question No: 24 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183) rep**

Question No: 25 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 27 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424) rep**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 28 (Marks: 1) - Please choose one **(Diagram is missing)**
In the circuit diagram of 3-bit synchronous counter shown above, The red rectangle would be replaced by which gate?
► **AND**
► OR
► NAND
► XNOR

Question No: 29 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2n (2 raise to power n)
► n2 (n raise to power 2)

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Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

- ► FIFO memory
- ► **LIFO memory (Page 429) rep**
- ► Flash Memory
- ► Bust Flash Memory

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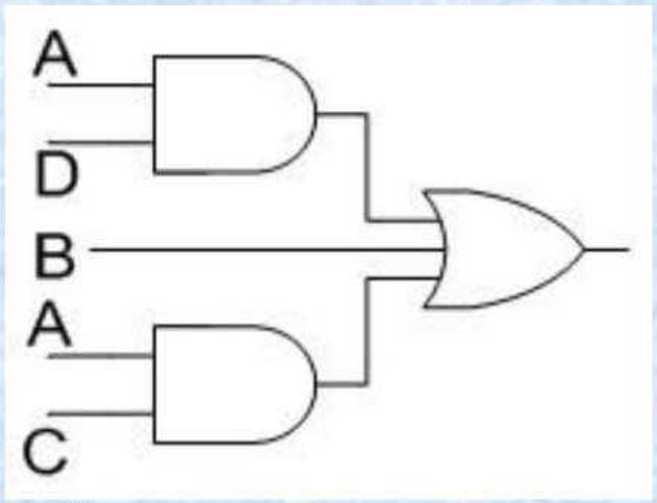
FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The diagram given below represents _____



- Demorgans law
- Associative law
- Product of sum form
- **Sum of product form (Page 78) rep**

Question No: 2 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "+7"

- **0000 (Page 34) rep**
- 1001
- 1000
- 1111

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Question No: 3 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

► = 0, Cout = 0
► **= 0, Cout = 1 (Page 135) rep**
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 5 (Marks: 1) - Please choose one
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 6 (Marks: 1) - Please choose one
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 7 (Marks: 1) - Please choose one
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.

► **TRUE (Page 182)**
► FALSE

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____

► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

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Question No: 9 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 10 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 11 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

- ► GATED FLIP-FLOPS
- ► PULSE TRIGGERED FLIP-FLOPS
- ► POSITIVE-EDGE TRIGGERED FLIP-FLOPS
- ► **NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267) rep**

Question No: 12 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319) rep**

Question No: 13 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____

- ► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
- ► MOD-10 AND MOD-6 COUNTERS
- ► MOD-10 AND MOD-2 COUNTERS
- ► **A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299) rep**

Question No: 14 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
- ► **The next state of a given present state (Page 371) rep**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

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Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.

- ► Mealy machine
- ► **Moore Machine (Page 332) rep**
- ► State Reduction table
- ► State Assignment table

Question No: 16 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

- ► 3
- ► **4 (Page 281)**
- ► 7
- ► 10

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► **Parallel data to serial (Page 356) rep**
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

- ►**Parallel in / Serial out shift register (Page 356)**
- ►Serial in / Parallel out shift register
- ►Parallel in / Parallel out shift register
- ►Serial in / Serial Out shift register

Question No: 19 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

Question No: 20 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356)**

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Question No: 21 (Marks: 1) - Please choose one
5-BIT JOHNSON COUNTER SEQUENCES THROUGH ____ STATES

► 7
► **10 (Page 354) rep**
► 32
► 25

Question No: 22 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►**Ring counter (Page 355)**

Question No: 23 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 24 (Marks: 1) - Please choose one
If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 25 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 26 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.
► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

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Question No: 27 (Marks: 1) - Please choose one **(Diagram is missing)**
In the circuit diagram of 3-bit synchronous counterThe red rectangle, shown above would be replaced which gate?

► AND
► OR
► NAND
► XNOR

Question No: 28 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------
—
► THE FLOP-FLOP IS TRIGGERED
► Q=0 AND Q'=1
► Q=1 AND Q'=0
► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)**

Question No: 29 (Marks: 1) - Please choose one
A frequency counter _____

► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301) rep**
► Counts high and low range of given clock pulse
► None of given options

Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

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